

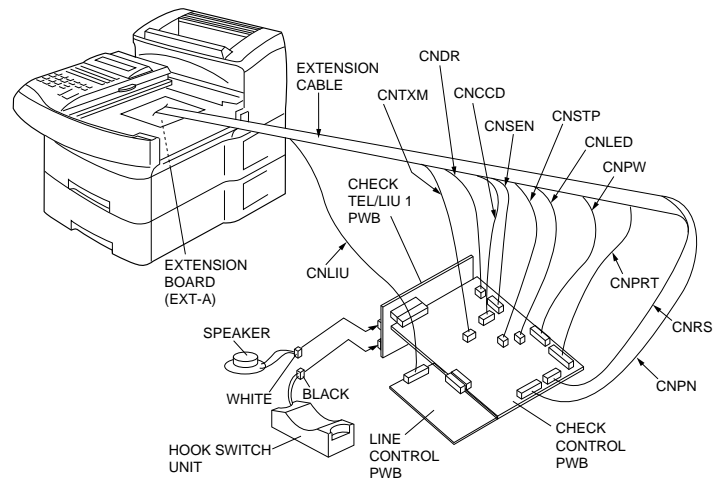


[For inspection of TEL/LIU 1 PWB]

- 1) Remove the left side panel.
  - 2) Remove the inner tray from the unit, and remove the control/line control PWB.
  - 3) Mount the extension board (EXT-A) in the place where the control/line control PWB has been removed.
  - 4) Connect the cables from the unit to the connectors (A side) (CNSENA, CNCCDA, CNPWA, CNPRTA, CNRSA, CNPNA, CNTXMA, CNLEDA, CNSTPA, CNDRA, CNLIUSA) of extension board (EXT-A) as on the control/line control PWB.
  - 5) Connect the extension cables (11 types) to the connectors (B side) of extension board (EXT-A).
  - 6) Remove the ROM cover of inner tray, pull out the extension cables (11 types) from the ROM replacing window, and mount the inner tray on the unit.
- \* When checking the TEL/LIU 1 PWB, the extension cable (QCNW-4608SCZZ) and extension board (EXT-B) are not used.
- 7) Connect the TEL/LIU 1 PWB to be checked to the connector (CNLIU) of control PWB.
  - 8) Connect the extension cables (11 types) pulled out from the unit to the control/line control PWB.
  - 9) Fit the speaker unit and hook switch unit of left upper panel as an assembly in the TEL/LIU 1 PWB to be checked.

Cable parts code	Connector	Remark
QCNW – 4597SCZZ	CNCCD	Control PWB
QCNW – 4598SCZZ	CNSEN	
QCNW – 4599SCZZ	CNPW	
QCNW – 4600SCZZ	CNRS	
QCNW – 4601SCZZ	CNPN	
QCNW – 4602SCZZ	CNLED	
QCNW – 4604SCZZ	CNSTP	
QCNW – 4605SCZZ	CNROL	
QCNW – 4606SCZZ	CNTXM	
QCNW – 4609SCZZ	CNPRT	
QCNW – 4828SCZZ	CNLIU1	Line control PWB

Extension board connection diagram (TEL/LIU 1 PWB)

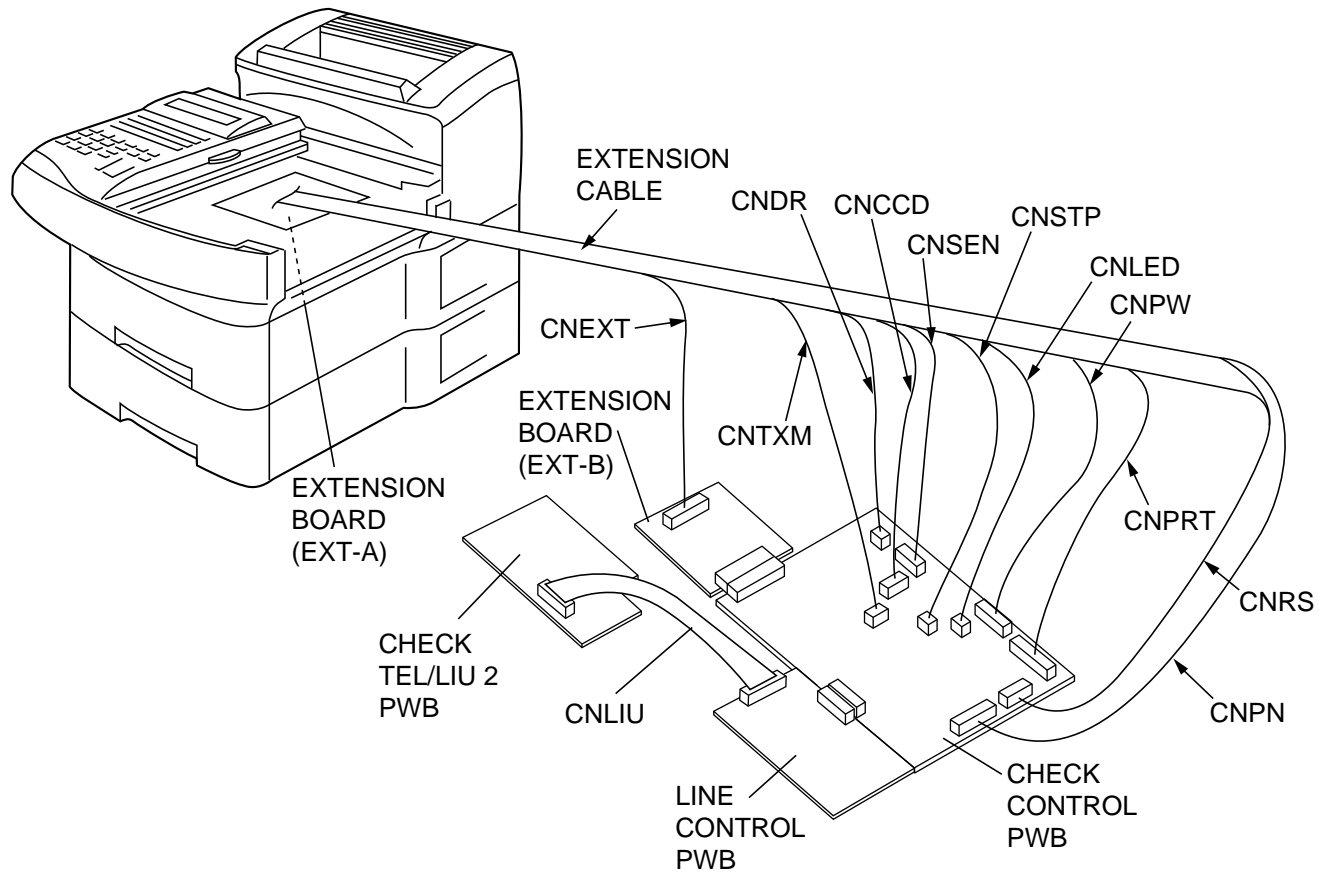


[For inspection of TEL/LIU 2 PWB]

- 1) Remove the left side panel.
  - 2) Remove the inner tray from the unit, and remove the control/line control PWB.
  - 3) Mount the extension board (EXT-A) in the place where the control/line control PWB has been removed.  
At that time, the connector (CNLIU) of extension board (EXT-A) must be inserted into the TEL/LIU 2 PWB.
  - 4) Connect the cables from the unit to the connectors (A side) (CNSENA, CNCCDA, CNPWA, CNPRTA, CNRSA, CNPNA, CNTXMA, CNLEDA, CNSTPA, CNDRA) of extension board (EXT-A) as on the control/line control PWB (Non connection CNLIUSA).
  - 5) Connect the extension cables (11 types) to the connectors (B side) of extension board (EXT-A).
- \* When checking the TEL/LIU 2 PWB, the extension cable (QCNW-4828SCZZ) and extension board (EXT-A) are not connect.
- 6) Remove the ROM cover of inner tray, pull out the extension cables (11 types) from the ROM replacing window, and mount the inner tray on the unit.
  - 7) Connect the extension cable (QCNW-4608SCZZ) pulled out to the connector (CNEXTB) of extension board (EXT-B).
  - 8) Connect the extension board (EXT-B) to the connector (CNLIU) of control PWB.
  - 9) Connect the extension cables (10 types (except CNEXTB)) pulled out from the unit to the control/line control PWB.
  - 10) Connect the CNLIU1 connector of line control PWB to the CNLIU connector of TEL/LIU 2 PWB through the extension cable (QCNW-4828SCZZ).

Cable parts code	Connector	Remark
QCNW – 4597SCZZ	CNCCD	Control PWB
QCNW – 4598SCZZ	CNSEN	
QCNW – 4599SCZZ	CNPW	
QCNW – 4600SCZZ	CNRS	
QCNW – 4601SCZZ	CNPN	
QCNW – 4602SCZZ	CNLED	
QCNW – 4604SCZZ	CNSTP	
QCNW – 4605SCZZ	CNROL	
QCNW – 4606SCZZ	CNTXM	
QCNW – 4608SCZZ	CNEXTB	
QCNW – 4609SCZZ	CNPRT	Control PWB
QCNW – 4828SCZZ	CNLIU1	Line control PWB

## Extension board connection diagram (TEL/LIU 2 PWB)



NO.	PARTS CODE	DESCRIPTION	Q'TY	PRICE RANK
1	QCNCM7014SC0H	CONNECTOR 8pin (CNCCDA, CNCCDB)	2	AB
2	QCNCM7014SC0F	CONNECTOR 6pin (CNSENA, CSENENB)	2	AB
3	QCNCM7014SC1B	CONNECTOR 12pin (CNPWA, CNPWB)	2	AD
4	QCNCM2482SC1H	CONNECTOR 18pin (CNRSA, CNRSB)	2	AE
5	QCNCM2482SC2D	CONNECTOR 24pin (CNPNA, CNPNB)	2	AB
6	QCNCM2401SC0B	CONNECTOR 2pin (CNLEDA, CNLEDB)	2	AA
7	QCNCM7014SC0B	CONNECTOR 2pin (CNSTPA, CNSTPB)	2	AD
8	QCNCM705BAF06	CONNECTOR 2pin (CNDRA, CNDRB)	2	AB
9	QCNCM7014SC0D	CONNECTOR 4pin (CNTXMA, CNTXMB)	2	AB
10	QCNCM2482SC2F	CONNECTOR 26pin (CNEXTA, CNEXTB)	2	AG
11	QCNCM2524SC3B	CONNECTOR 32pin (CNPRTA, CNPRTB)	2	AP
12	QCNCW2436SC2F	CONNECTOR 26pin (CNLIUA)	1	AG
13	QCNCM2531SC2F	CONNECTOR 26pin (CNLIUB)	1	AK
14	QCNCM2558SC2F	CONNECTOR 26pin (CNLIUSA, CNLIUSB)	2	AK
15	QCNW-4597SCZZ	CABLE 8pin (CNCCD)	1	AN
16	QCNW-4598SCZZ	CABLE 6pin (CNSEN)	1	AL
17	QCNW-4599SCZZ	CABLE 6pin (CNPW)	1	AQ
18	QCNW-4600SCZZ	CABLE 18pin (CNRS)	1	AU
19	QCNW-4601SCZZ	CABLE 24pin (CNPN)	1	AX
20	QCNW-4602SCZZ	CABLE 2pin (CNLED)	1	AG
21	QCNW-4604SCZZ	CABLE 2pin (CNSTP)	1	AG
22	QCNW-4605SCZZ	CABLE 2pin (CNDR)	1	AG
23	QCNW-4606SCZZ	CABLE 4pin (CNTXM)	1	AK
24	QCNW-4608SCZZ	CABLE 26pin (CNEXT)	1	AX
25	QCNW-4609SCZZ	CABLE 32pin (CNPRT)	1	BD
26	QCNW-4828SCZZ	CABLE 26pin (CNLIU)	1	AX

## 2-2. Optical adjust plate

### 1. General

This procedure defines the in-field adjustment method for the FO-6500 series scanner optical system – CCD, lenses, mirrors, etc. – which may be required when the optical system is removed for servicing. This adjustment needs the use of a special in-field scanner optical system adjust tool and a dual beam oscilloscope.

### 2. Adjustment

- 1) Remove the left cabinet, scanner front cover, inner tray, and printer front cover. As shown in Fig. 6, incline the scanner unit.
- 2) Connect the oscilloscope as follows: –  
CH1 to video signal (AVO) on control board  
CH2 to sync signal (PHIT) on control board  
GND to test point ground (DG) on control board.
- 3) Turn machine power on.
- 4) Select the optical adjust mode of diagnostics then press the START/COPY key.
- 5) Open Operation Panel. Then unit the optical adjustment tool on the lower document guide. (Fig. 7)
- 6) Remove the lock paint of CCD board holding screws. Then loosen one screw at a time and adjust the location of the CCD board so that the CCD output is as shown in Fig. 2. Also ensure that the centre black level trough is delayed 528msec from the trigger sync signal FT (PHIT). See Fig. 5.

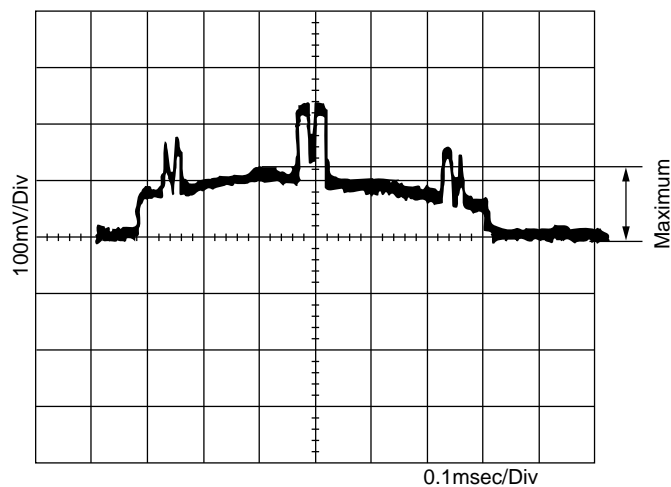


Fig. 1

Note: Above shows correct CCD output but focus need adjusting as in step 8.

- 7) If after adjusting CCD output in step 6) scope reads the same as in Fig. 2 run a test copy. (Focus should be OK)

Note: If the lens and lens holder have not been moved. You may skip step 8.

- 8) Remove the lock paint of lens. Adjust the location of the lens so that the difference between A and B of CCD output should be the largest, then secure the lens on that position. The output signal waveform must be symmetrical. After it has been complete, secure the screws with the lock paint. with this, lens focus adjustment is complete. (Fig. 2)

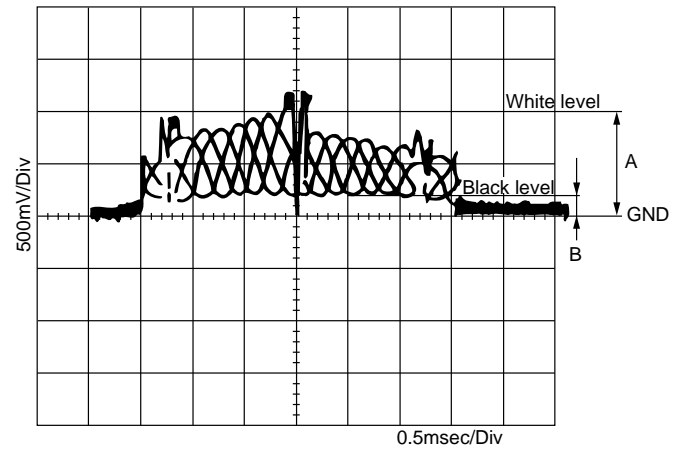


Fig. 2

- 9) Press STOP key again after completion of the adjustments. The mode is shifted to the diagnostic STANDBY MODE.

Notes:

- 1) Adjust the optical adjustment tool in the slant state as shown in Fig. 6. After the adjustment, the waveform will slightly vary if it is stood up as shown in Fig. 8.
- 2) Use the optical adjustment tool by pressing it in the arrow direction. If it is floated, the proper adjustment is impossible. (Fig. 3)

Optical adjustment tool

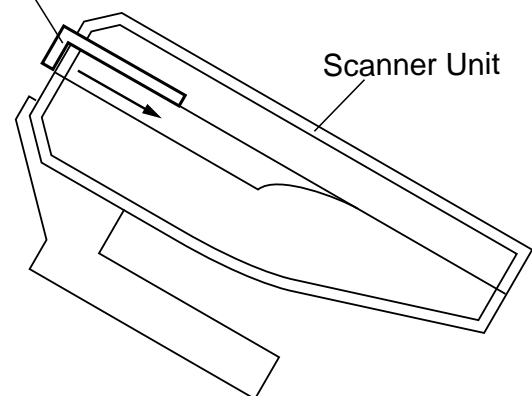


Fig. 3

### 3. Relationship of adjusting plate and oscilloscope output

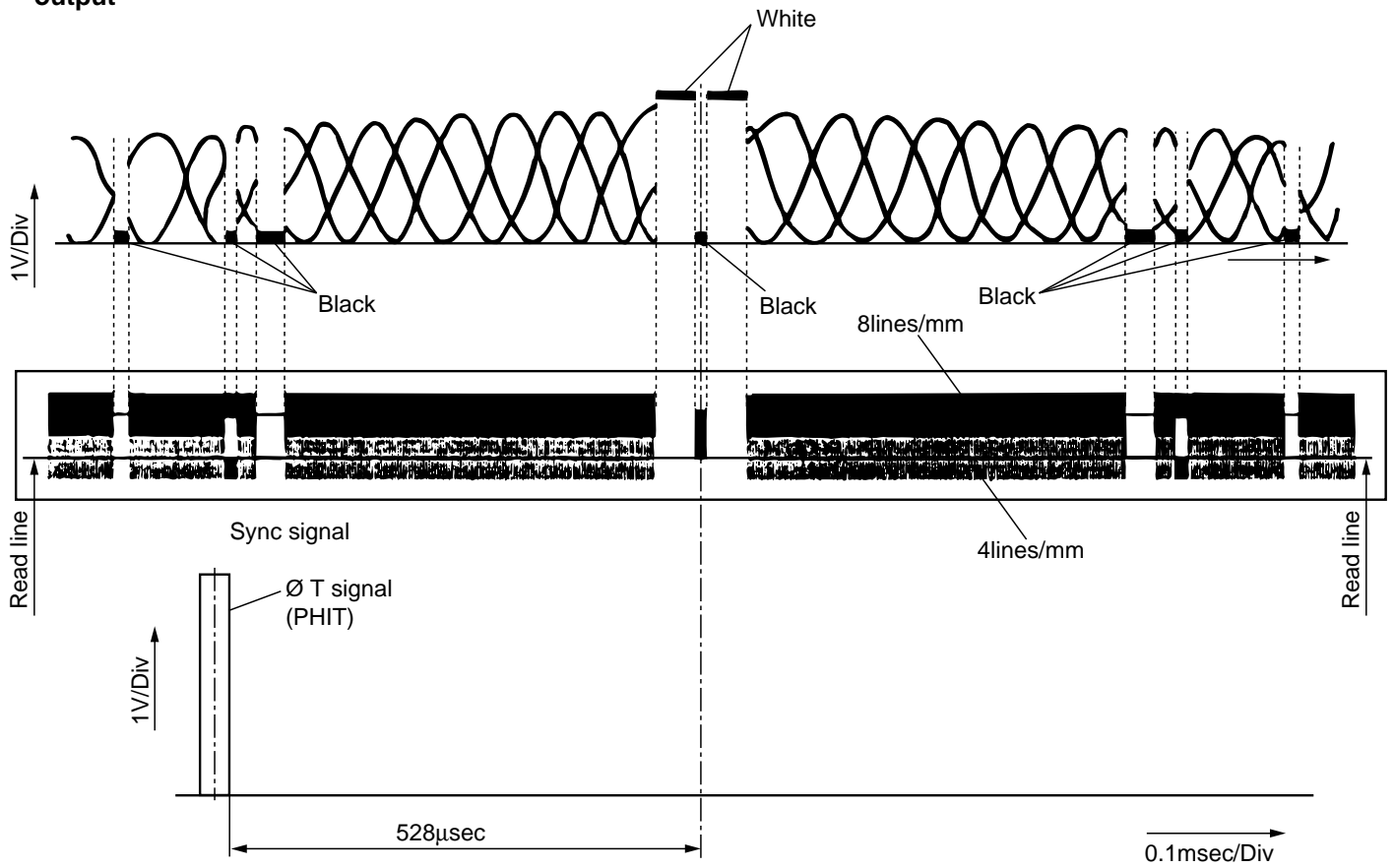


Fig. 4

Note: The CCD output must be adjusted to produce a white level at the center and black levels near the center and 8 lines/mm black and white pattern in other locations. Adjustment should be made so that the center of the white level signal is delayed 528msec from the sync signal PHIT. If this is not obtained the copy image may be shifted left or right causing incoplete scanning.

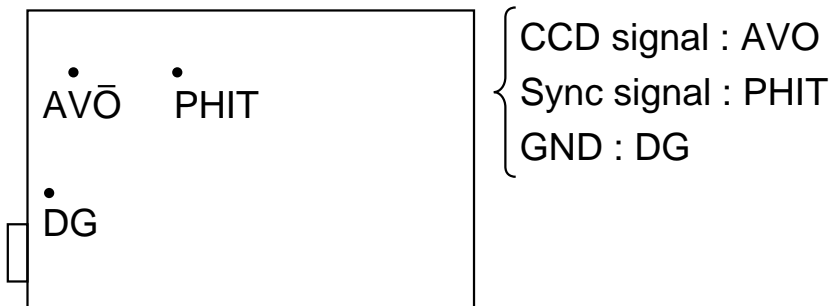


Fig. 5

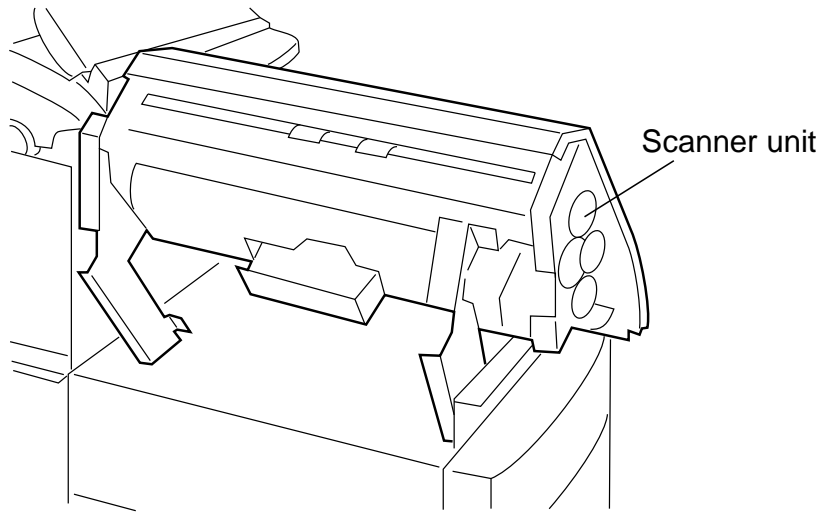


Fig. 6

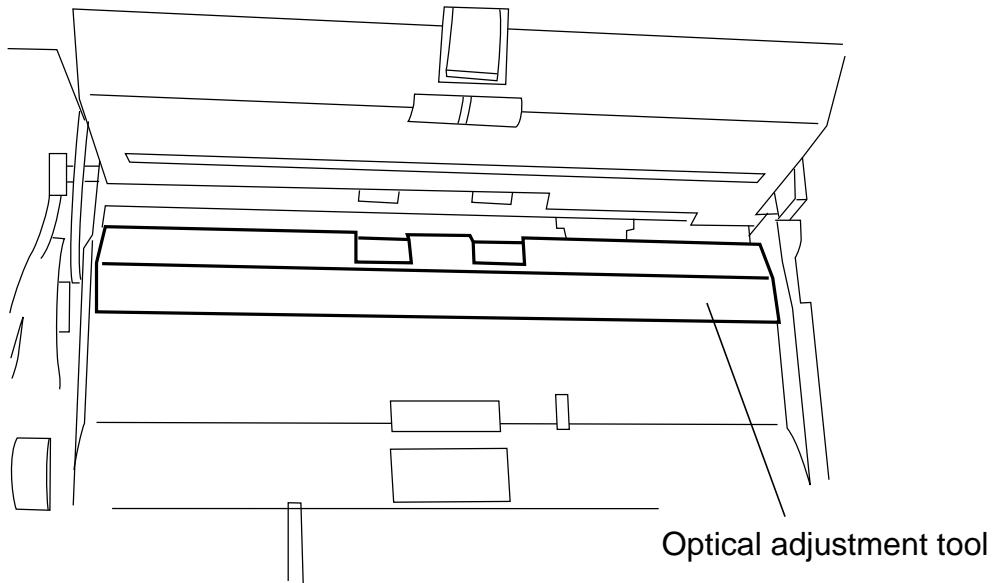


Fig. 7

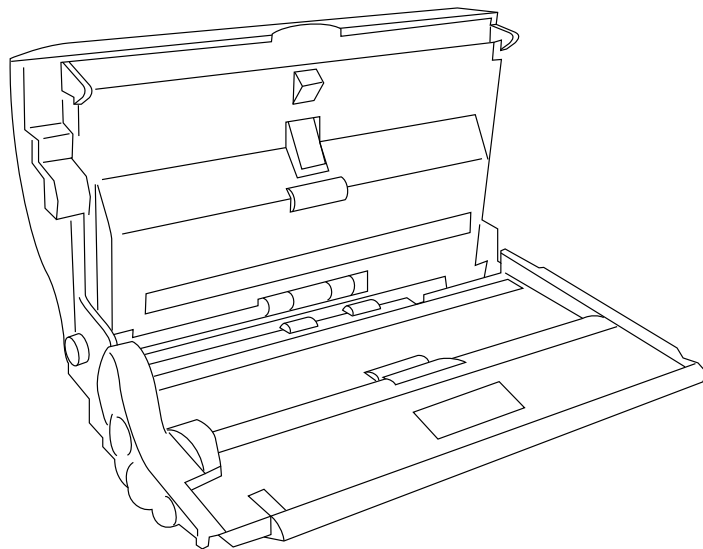
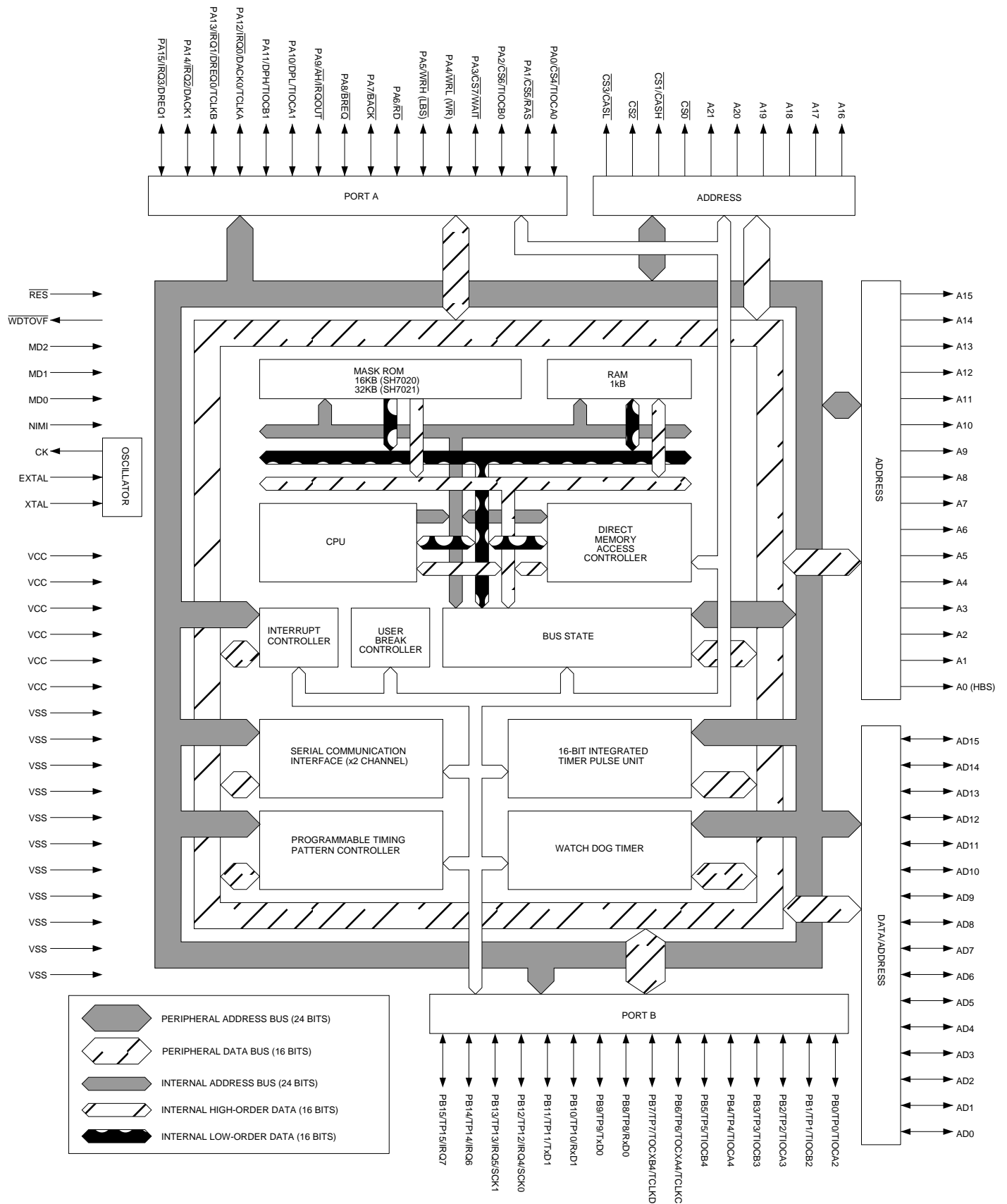


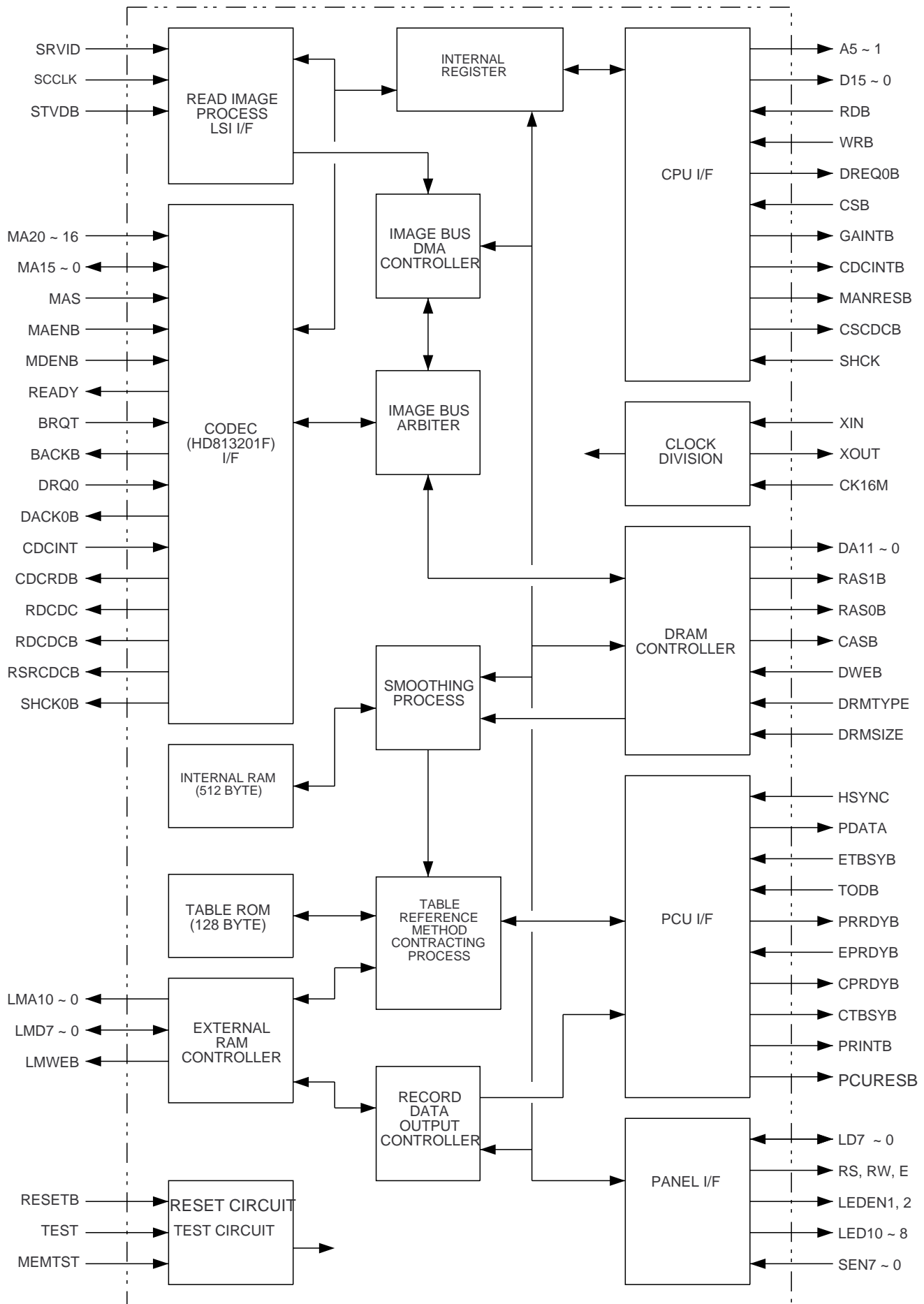
Fig. 8

[2] IC signal name

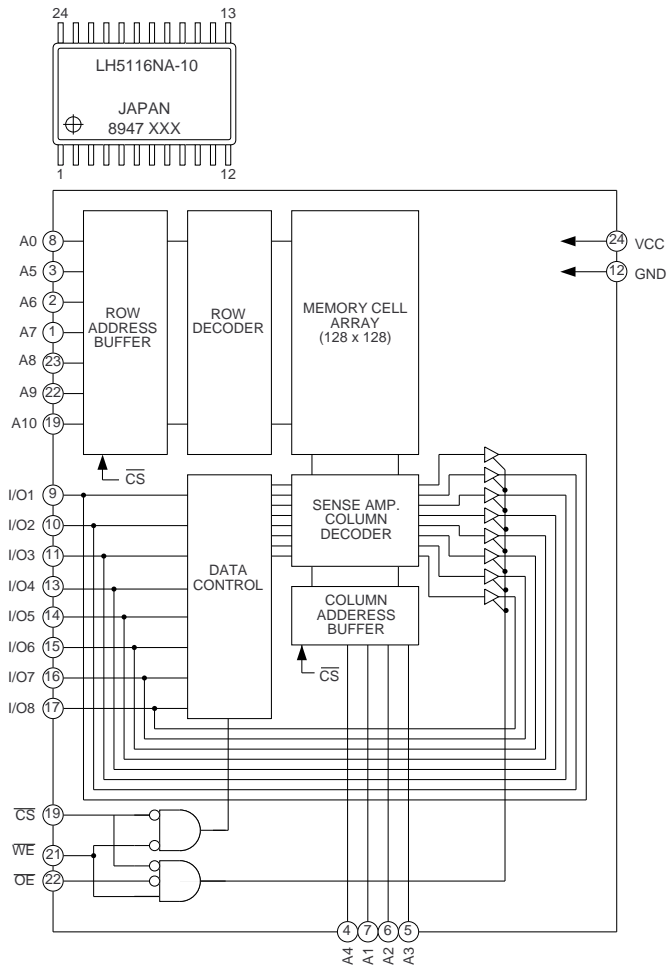
IC4, 13: VHi02120FAB0A



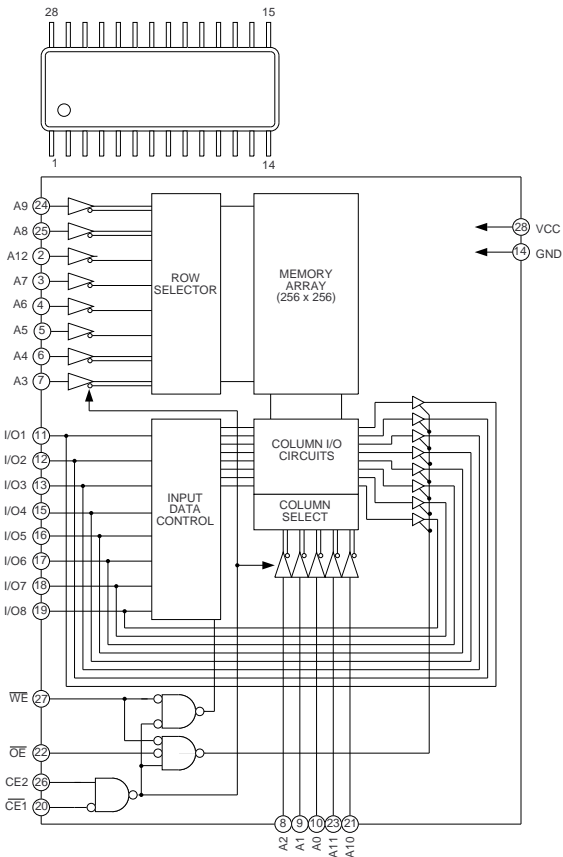
IC18: VHiLR38292/-1 (LR38292)



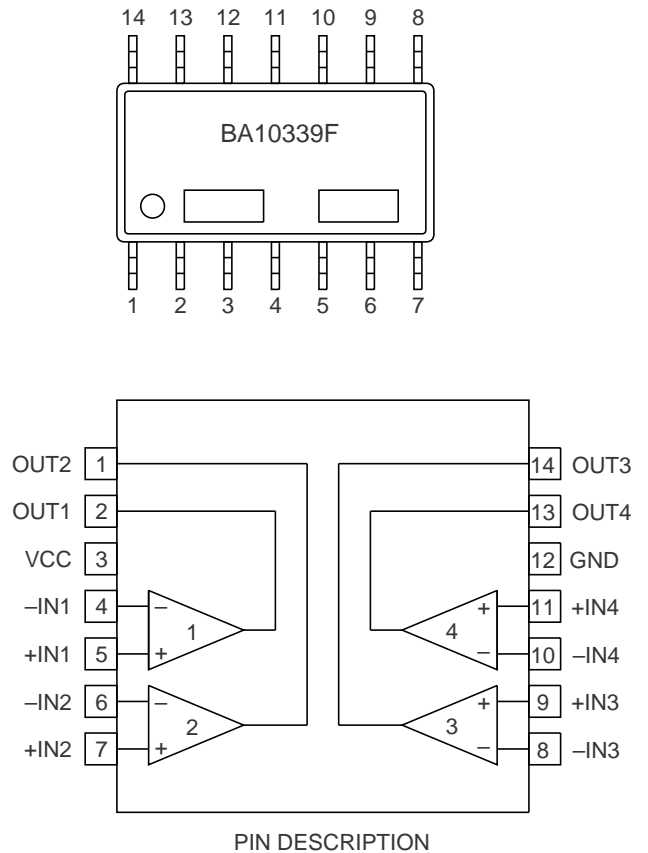
**IC22: VHiLH5116NA10 (LH5116NA-10)**



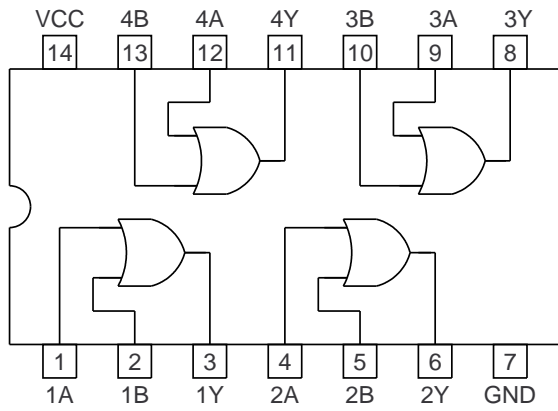
**IC23, 24: VHiLH5268TH10 (LH5268)**



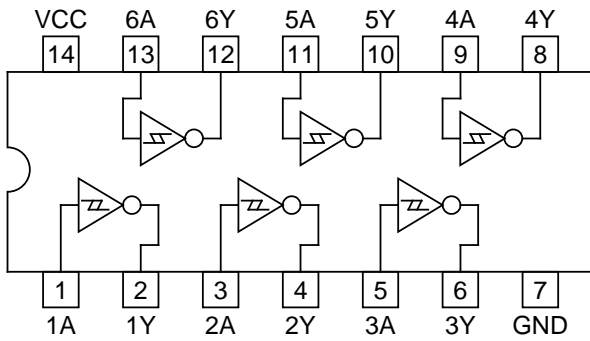
**IC130: VHiBA10339F-1 (BA10339F)**



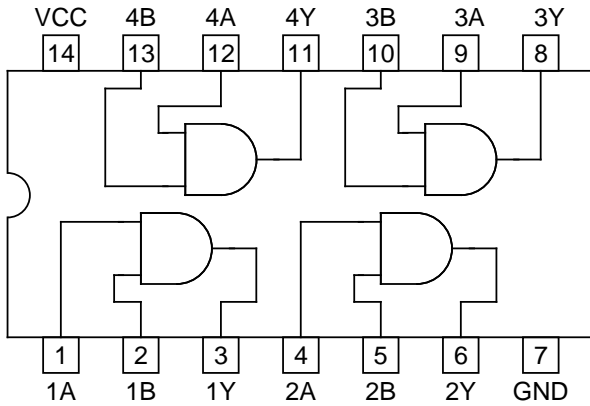
**IC113: VHiMC74HC32F- (MC74HC32AF)**



**IC109: VHiMC74HC14F- (MC74HC14AF)**

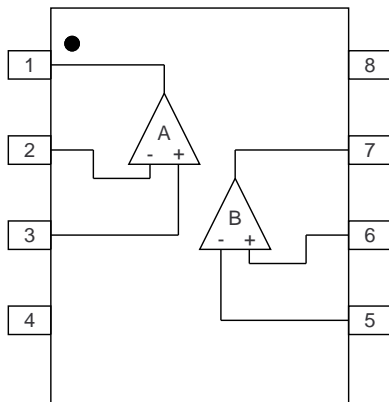


**IC121, 122: VHiMC74HC08F- (MC74HC08AF)**

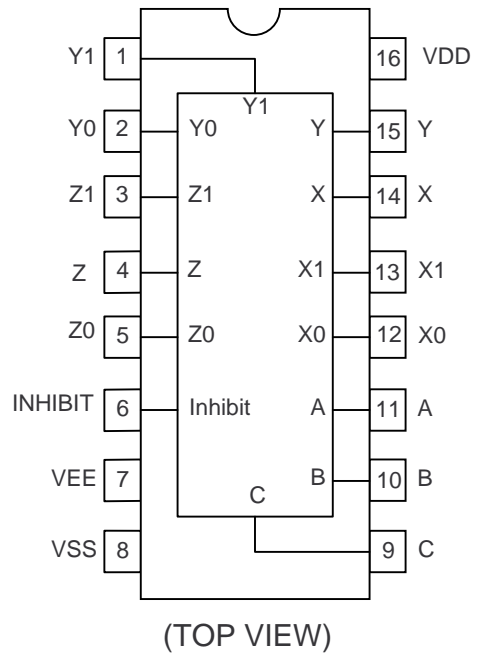


**IC111: VHiNJM2902M-1 (NJM2902M)**

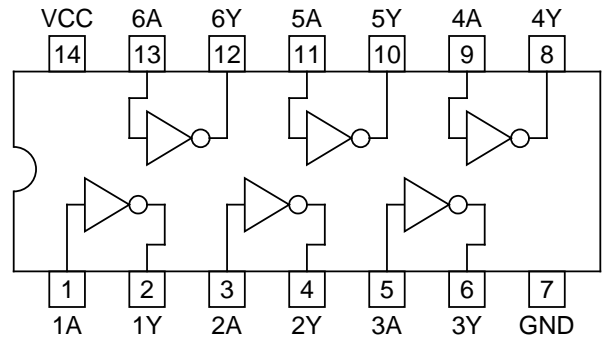
**IC115: VHiNJM2904M-1 (NJM2904M)**



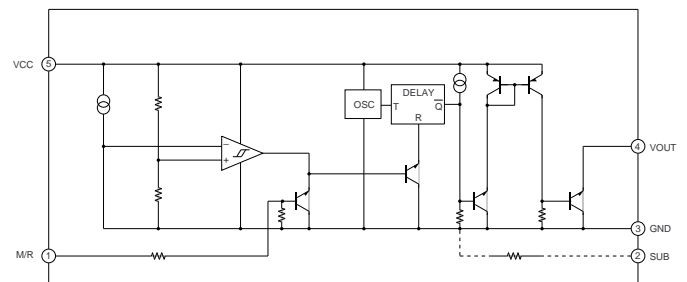
**IC119: VHiBU4053BCF1 (BU4053BCF)**



**IC114, 120: VHiMC74HC04F- (MC74HC04AF)**



**IC110: VHiPST596CMT1 (PST596CNR)**





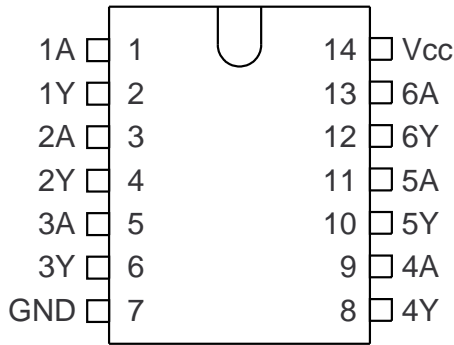
## IC25: VHiTLS1049/-1 (TLS1049)

1	SEL ●	AVCC	30
2	VREF+	DVCC	29
3	AVO	PGST	28
4	VRLM	B-/H	27
5	VRHF	GTW-	26
6	PHCAP	PHIBL-	25
7	CLPB	B5	24
8	CLPF	B4	23
9	SHCAP	B3	22
10	VO	B2	21
11	M-EX	B1	20
12	VI	B0	19
13	VC	ADCK	18
14	VH	PHISH-	17
15	AGND	DGND	16

No	Terminal Name	Type	Function
1	SEL	IN D	Input pre-amp gain switching terminal. L: Internal, H: External
2	VREF+	OUT A	VREF upper voltage monitor terminal for AD.
3	AVO	OUT A	AD input monitor terminal.
4	VRLM	IN A	In the binary mode, upper voltage minimum limit setting terminal for AD.
5	VRHF	IN A	In the halftone mode, upper voltage setting terminal for AD.
6	PHCAP	I/O A	External capacitor connecting terminal for AGC.
7	CLPB	IN A	DC clamp, offset canceler, and signal input.
8	CLPF	OUT A	Sample hold buffer output.
9	SHCAP	I/O A	For sample hold, external capacitor connecting terminal.
10	VO	OUT A	Input pre-amp output
11	M-EX	IN A	When setting the external gain, minus input of input pre-amp.
12	VI	IN A	Video signal input.
13	VC	I/O A	Internal reference voltage smoothing terminal. External capacitor 1mF connection.
14	VH	OUT A	Voltage output for VRHF and VRLM generation. Terminal voltage: 3.65V
15	AGND	PS -	Analog GND power supply.
16	DGND	PS -	Digital GND power supply.
17	PHISH	IN D	Control input for sample hold. L: Sample, H: Hold
18	ADCK	IN D	Reference clock input for AD converter.
19	B0	OUT D	AD converter data output B0. LSB
20	B1	OUT D	AD converter data output B1.
21	B2	OUT D	AD converter data output B2.
22	B3	OUT D	AD converter data output B3.
23	B4	OUT D	AD converter data output B4.
24	B5	OUT D	AD converter data output B5. MSB
25	PHIBL	IN D	Control input for DC clamp. L: Clamp
26	GTW	IN D	Binary setting voltage switching control input for AGC. H: Binary minimum limit, L: AVO
27	B/H	IN D	Halftone, binary setting voltage switching terminal for AGC. H: Halftone, L: Binary minimum limit, AVO
28	PGST	IN D	External capacitor discharge control input for AGC. L: Discharge
29	DVCC	PS -	Digital VCC power supply.
30	AVCC	PS -	Analog VCC power supply.

(Note 16) The abbreviations in the column of "Type" are as follows; IN: Input, OUT: Output, I/O: Input/Output, A: Analog, D: Digital, PS: Power supply pin.

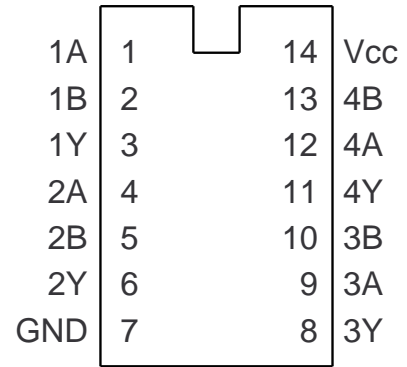
**IC106, 118: VHiALS04BNS-1 (SN74ALS04BNS)**



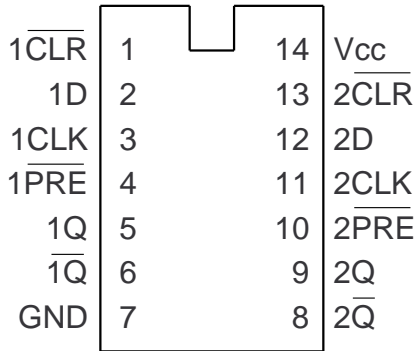
**IC107, 108: VHiALS32NS/-1 (SN74ALS32NS)**

**IC101, 132: VHiALS08NS/-1 (SN74ALS08NS)**

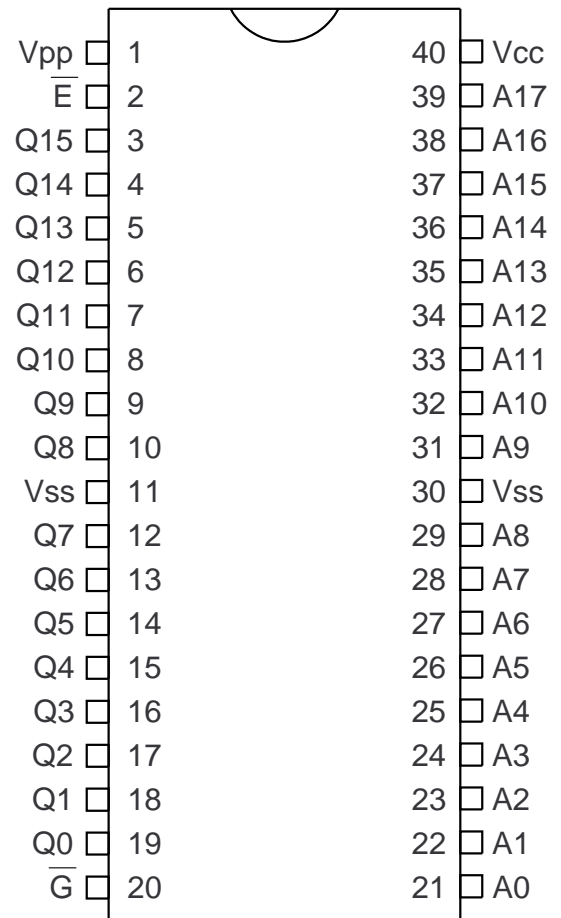
**IC133: VHiALS20ANS-1 (SN74ALS20ANS)**



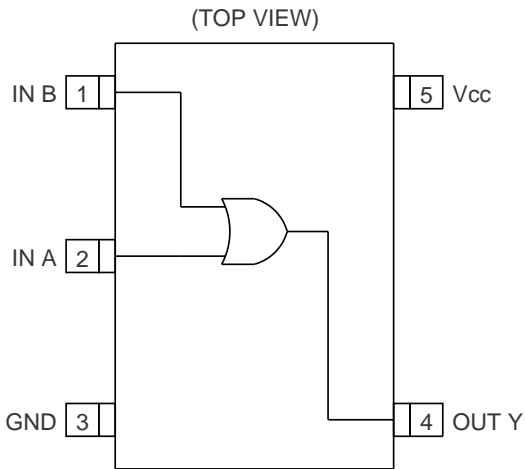
**IC102, 117: VHiALS74ANS-1 (SN74ALS74ANS)**



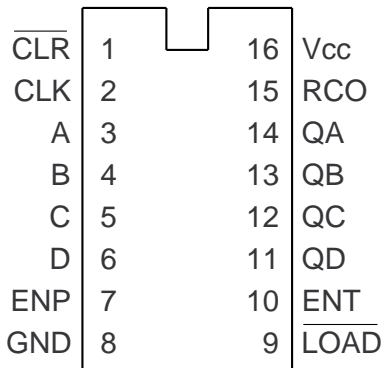
**IC10: VHiM27C400210 (M27C4002-10F1)**



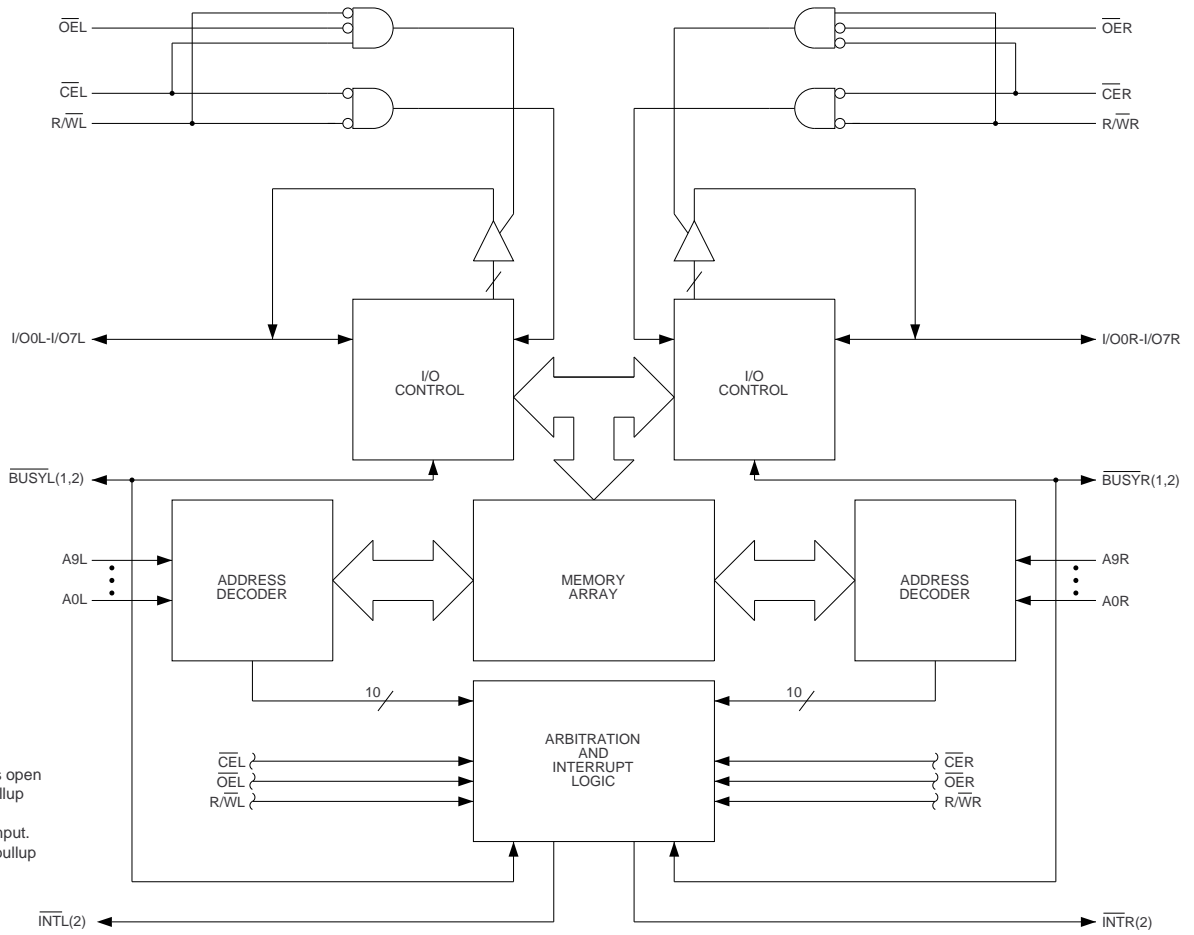
**IC104: VHiTC7SH32FU/ (TC7SH32FU)**



**IC1: VHiALS163BNS/ (SN74ALS163BNS)**



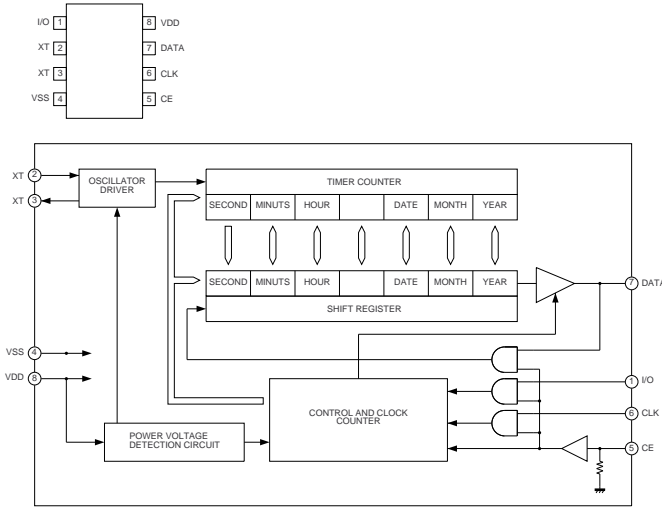
**IC16: VHiiDT7130-55 (IDT7130SA55PF)**  
**IC17: VHiiDT7140-55 (IDT7140SA55PF)**



- NOTES:  
 1. IDT7130(MASTER): $\overline{\text{BUSY}}$  is open drain output and requires pullup resistor of 270 $\Omega$ .  
 IDT7140(SLAVE): $\overline{\text{BUSY}}$  is input.  
 2. Open drain output:requires pullup resistor of 270 $\Omega$ .

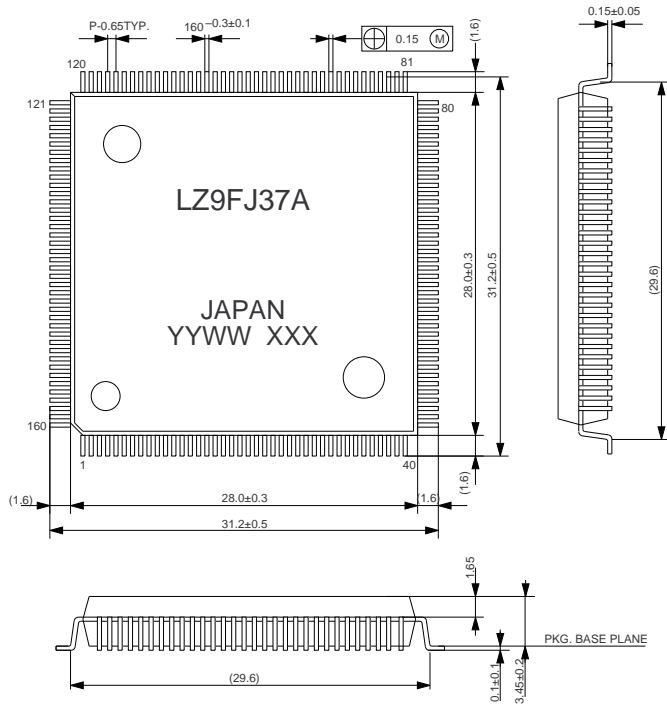
$\overline{\text{CEL}}$	1	48	Vcc
R/WL	2	47	$\overline{\text{CER}}$
$\overline{\text{BUSYL}}$	3	46	R/WR
INTL	4	45	$\overline{\text{BUSYR}}$
$\overline{\text{OEL}}$	5	44	INTR
A0L	6	43	$\overline{\text{OER}}$
A1L	7	42	A0R
A2L	8	41	A1R
A3L	9	40	A2R
A4L	10	39	A3R
A5L	11	38	A4R
A6L	12	37	A5R
A7L	13	36	A6R
A8L	14	35	A7R
A9L	15	34	A8R
I/O0L	16	33	A9R
I/O1L	17	32	I/O7R
I/O2L	18	31	I/O6R
I/O3L	19	30	I/O5R
I/O4L	20	29	I/O4R
I/O5L	21	28	I/O3R
I/O6L	22	27	I/O2R
I/O7L	23	26	I/O1R
GND	24	25	I/O0R

**IC127: VHiNJU6355E-1 (NJU6355E)**



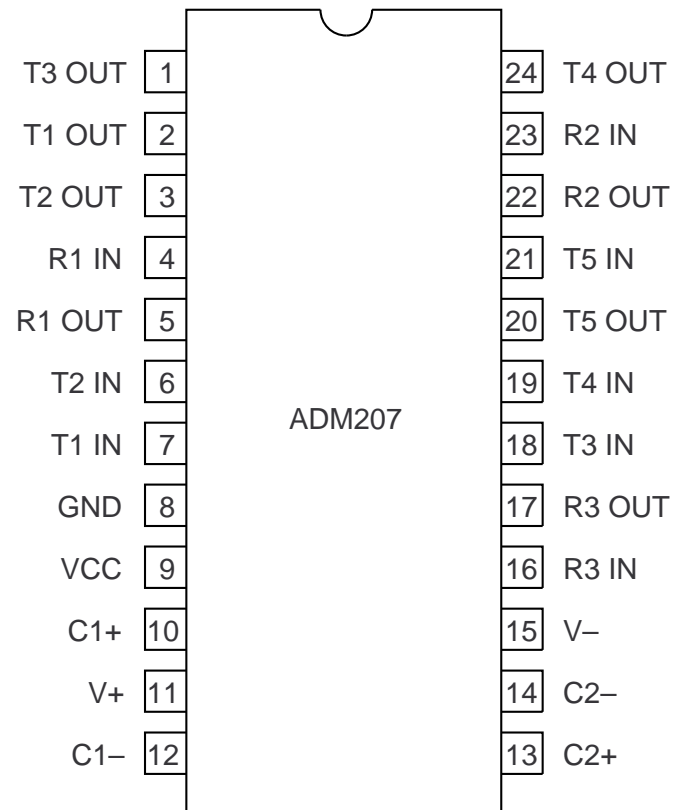
No.	Function	Description															
1	I/O	DATA pin I/O select pin "H": Data input "L": Data output When, however, CE pin is in "L", DATA pin is in high impedance															
2	XT	Crystal oscillator connection pin (f=32.768KHz)															
3	XT	For the capacity of Cg and Cd, refer to the series composition table															
5	CE	Chip enable input pin (built-in pull-down resistor), "H": DATA pin allows data input/output "L": DATA pin is in high impedance															
6	CLK	Clock input pin: Data are inputted or output in synchronization with this clock When, however, CE pin is in "L", DATA pin is in high impedance															
7	DATA	Serial timer data I/O pin <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>I/O</th> <th>CE</th> <th>DATA pin</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>Input</td> </tr> <tr> <td>L</td> <td>H</td> <td>Output</td> </tr> <tr> <td>H</td> <td>L</td> <td>High impedance</td> </tr> <tr> <td>L</td> <td>L</td> <td>High impedance</td> </tr> </tbody> </table>	I/O	CE	DATA pin	H	H	Input	L	H	Output	H	L	High impedance	L	L	High impedance
I/O	CE	DATA pin															
H	H	Input															
L	H	Output															
H	L	High impedance															
L	L	High impedance															
8	VDD	Power pin +5V															
4	VSS	Power pin GND															

**IC14: VHiLZ9FJ37-1 (LZ9FJ37A)**



**RS232C I/F PWB**

**IC1: VHiADM207AN-1 (ADM207AM)**



MEMO